IN THE CLAIMS:

Please amend claims 1-7, 9-16 and cancel claims 8 and 17 without prejudice as follows:

1. (Currently Amended) A debugging apparatus comprising:

a processor core operated by a program stored in a program memory to read ~~a~~ data stored in ~~a~~ data memory or write ~~a~~ data to data memory;

a debugger controller for performing ~~a~~ debugging on the processor ~~core~~ upon receipt of a command from a host computer and outputting a data break point address; and

a memory break controller for observing an address of ~~a~~ data memory ~~used~~ accessed by the processor ~~core~~, recognizing ~~an~~ the accessed address as ~~a~~ the break point address, ~~to~~ outputting a first break signal to the debugger controller and the processor ~~core~~ to suspend ~~the~~ operation of the processor ~~core~~, ~~when the address is sensed to be identical,~~ and transmitting ~~a corresponding~~ the accessed address and data stored at the accessed address to the host computer through the debugger controller~~.~~, wherein if data is read from the accessed address by the processor, the address and corresponding data of each data memory location subsequently accessed by the processor is output to the host computer until the address identical to the breakpoint address is written to.

2. (Currently Amended) The apparatus of claim 1, wherein the data memory stores a data value outputted from the processor ~~core~~.

3. (Currently Amended) The apparatus of claim 1, wherein after the memory break controller transmits ~~an~~ the accessed address and ~~a~~ corresponding data ~~recognized as a break point~~, the break point controller activates ~~an~~ operation of the processor ~~core,~~ and outputs the ~~used~~ accessed address and ~~the~~ data of the data memory to the host computer through the debugger controller until a second break signal is output~~ted again~~.

4. (Currently Amended) The apparatus of claim 3, wherein the host computer recognizes a data flow and change ~~by~~ of the address and the data output~~ted~~ from the memory break controller.

5. (Currently Amended) The apparatus of claim 1, wherein the memory break controller comprises:

a memory break control register ~~being~~ activated by the break point address and ~~the~~ a control signal ~~inputted~~ from the debugger controller;

an address register for storing the break point address input~~ted~~ from the memory break control register;

an address comparator for comparing the address of the data memory currently ~~used~~ accessed by the processor ~~core~~ and the break point address stored in the address register;

a data register for storing ~~the~~ data stored at ~~of~~ the break point address ~~stored in the address register~~; and

a data comparator for comparing the data ~~of~~ stored at the currently accessed address ~~outputted from~~ of the data memory and the data ~~of the break point address~~ stored in the data register.

6. (Currently Amended) The apparatus of claim 5, wherein the memory break control register comprises:

a memory break enable flag for activating the memory break controller;

a data check flag ~~for sensing~~ enabled when data is read from an address of the data memory which is identical to the break point address ~~stored in the address register, and being enabled when the content of the data of the sensed address is outputted~~; and

an address trace check flag ~~for being~~ enabled when ~~the content of~~ data is read from the address of the data memory which is identical to the break point address ~~stored in the address register is outputted~~.

7. (Currently Amended) The apparatus of claim 6, wherein when the address trace check flag is enabled, ~~it outputs~~ the addresses and corresponding data of every memory ~~which are read from or written in~~ location accessed by the processor ~~core before~~ are output until the content of the break address is updated.

8. (Canceled)

9. (Currently Amended) A debugging method comprising the steps of:

outputting ~~an address of a data memory to be observed, that is~~ a break point address of data memory to be observed and a break enable signal~~,~~ when a processor is switched to a debugging mode;

storing the outputted break point address~~,~~ and operating the processor in a general operation state;

comparing the stored break point address and the address of the data memory currently ~~used~~ accessed by the processor ~~core, while the process is being operated~~;

outputting a break signal to suspend operation of the processor ~~core,~~ if the address of the data memory currently ~~used~~ accessed by the processor ~~core~~ and the stored break point address are identical ~~to each other~~; ~~and~~

suspending operation of the processor ~~core by~~ in response to the output~~ted~~ break signal ~~and switching the processor to a debugging mode to debug the program~~.

transmitting the currently accessed address and corresponding data; and

re-activating the operation of the processor and outputting the address and corresponding data of each data memory location accessed by the processor until another break signal is output.

10. (Currently Amended) The method of claim 9, wherein ~~in the step of operating a~~ upon switching the processor to debugging mode, the processor is initialized by enabling~~,~~ a memory break enable flag of a memory break controller ~~is enabled according~~ in response to ~~an outputted~~ a break enable signal~~,~~ ~~and~~ a data check

flag and an address check flag are disabled, ~~in order to initialize the processor,~~ and ~~then~~ the break point address is stored.

11. (Currently Amended) The method of claim ~~9~~ 10, ~~wherein the step of outputting a break signal comprises~~ further comprising:

~~a step in which when~~ determining that an address of the data memory currently ~~used~~ accessed by the processor ~~core~~ and the stored break point address are identical ~~to each other, it is;~~ ~~determined~~

determining whether the processor reads ~~the~~ data ~~stored~~ from ~~in~~ the ~~corresponding~~ currently accessed address or writes ~~a~~ data to the currently accessed address;

~~a step in which, in case of reading a data,~~ enabling the address trace check flag and the data check flag of the memory break control register ~~are enabled~~ if it is determined that data is read from the currently accessed address;

re-activating the operation of the processor;

~~a step in which the corresponding~~ comparing a subsequently accessed address of the data memory and the stored break point address ~~are compared again~~; and

~~a step in which,~~ if the ~~corresponding~~ subsequently accessed address of the data memory and the break point address are not identical ~~to each other~~, transmitting the ~~corresponding~~ subsequently accessed address and corresponding data ~~of the data memory are transmitted~~ to the host computer.

12. (Currently Amended) The method of claim 11, ~~wherein the step of comparing address comprises~~ further comprising:

~~a step in which, if~~ determining that the ~~corresponding~~ subsequently accessed address of the data memory and the break point address are identical ~~to each other,; it is determined~~

determining whether the processor reads ~~a~~ data from ~~stored in~~ the subsequently accessed ~~data memory of the corresponding~~ address or writes ~~a~~ data ~~in the data memory of the corresponding~~ to the subsequently accessed address; and

if it is determined that the processor writes ~~a step in which, in case of writing a~~ data to the subsequently accessed, the data check flag of the memory break controller is enabled and a break signal for suspending the processor ~~core~~ is outputted.

13. (Currently Amended) The method of claim 12, wherein, ~~in case of reading a~~ if it is determined that the processor reads data ~~upon judgement~~ from the subsequently accessed address, ~~an address of~~ the next data memory ~~to be used~~ location accessed by the processor ~~core~~ and the break point address are compared.

14. (Currently Amended) The method of claim 11, wherein, ~~in case of writing a~~ if it is determined that the processor writes data ~~in the judging step~~ to the currently accessed address, the data check flag of the memory break controller is set and the operation of the processor ~~core is discontinued~~ suspended.

15. (Currently Amended) The method of claim 9, wherein, after ~~in the step of outputting a break signal, when~~ the operation of the processor core is suspended by the break signal, the address and data of the corresponding data memory are transmitted~~,~~ and ~~then~~ the operation of the processor core is re-activated ~~to output an address and a data of the data memory used by the processor core~~ until ~~a~~ another break signal is output~~ted again~~.

16. (Currently Amended) A debugging method for informing a data transition state, comprising:

~~a step in which when~~ switching a processor ~~is switched into~~ to a debugging mode~~, an~~ and outputting a break point address of a data memory to be observed~~, that is, a break point address,~~ and a break enable signal ~~are outputted~~;

~~a step in which~~ storing the ~~outputted~~ break point address ~~is stored~~;

~~a step in which~~ comparing the stored break point address and an address of a data memory currently ~~used~~ accessed by the ~~a~~ processor ~~core are compared~~;

~~a step in which, when~~ determining that the address of the data memory currently ~~used~~ accessed by the processor ~~core~~ and the stored break point address are identical ~~to each other, it is determined whether the processor core reads a data stored in the corresponding address or writes a data~~;

~~a step in which, in case of writing a~~ determining that the processor writes data ~~in a corresponding~~ to the accessed address, enabling a data check flag of a memory break controller ~~is enabled~~ and outputting a break signal for suspending operation of the processor ~~core is outputted~~;

~~a step in which, when the processor core is suspended by the outputted break signal,~~ outputting the accessed address and the corresponding data ~~of the corresponding data memory are outputted~~; and

~~a step in which~~ re-activating the operation of the processor ~~core is activated~~ and outputting the address and ~~the~~ corresponding data of ~~the~~ each data memory ~~used~~ locations subsequently accessed by the processor ~~are outputted~~ until ~~a~~ another break signal is output~~ted again~~.

17. (Canceled)